

CLAIMS:

- 106250-0814550
- Sub-1
1. A method of forming a capacitor comprising:
forming a first capacitor electrode over a substrate;
forming a second capacitor electrode over the substrate; and
forming a capacitor dielectric region intermediate the first and second capacitor electrodes, the capacitor dielectric region forming comprising:
forming a silicon nitride comprising layer over the first capacitor electrode;
forming a silicon oxide comprising layer over the silicon nitride comprising layer; and
exposing the silicon oxide comprising layer to an activated nitrogen species generated from a nitrogen-containing plasma effective to introduce nitrogen into at least an outermost portion of the silicon oxide comprising layer, and forming silicon nitride therefrom effective to increase a dielectric constant of the dielectric region from what it was prior to said exposing.
 2. The method of claim 1 comprising forming the capacitor dielectric region to comprise an inner silicon oxide comprising layer received on the first capacitor electrode, with the silicon nitride comprising layer being formed on the inner silicon oxide comprising layer.
 3. The method of claim 1 comprising forming the silicon oxide comprising layer on the silicon nitride comprising layer.

4. The method of claim 1 wherein said exposing and forming silicon nitride therefrom transforms only an outermost portion of said silicon oxide comprising layer to silicon nitride.

5. The method of claim 1 comprising forming the silicon oxide comprising layer on the silicon nitride comprising layer, the silicon oxide comprising layer including a portion which is everywhere received elevationally over the silicon nitride comprising layer, said exposing and forming silicon nitride therefrom transforming all of said portion to silicon nitride.

6. The method of claim 1 comprising forming the silicon oxide comprising layer on the silicon nitride comprising layer, the silicon oxide comprising layer including a portion which is everywhere received elevationally over the silicon nitride comprising layer, said exposing and forming silicon nitride therefrom transforming only an outermost part of said portion to silicon nitride.

7. The method of claim 1 wherein the forming silicon nitride therefrom comprises thermally annealing the substrate at a temperature of at least 600°C after the exposing.

8. A method of forming a capacitor comprising:

forming first capacitor electrode material over a semiconductor substrate;
forming a silicon nitride comprising layer over the first capacitor electrode,
the silicon nitride comprising layer comprising pinholes formed therein;
forming a silicon oxide comprising layer over the silicon nitride comprising
layer and effective to fill said pinholes with silicon oxide;
exposing the silicon oxide comprising layer to an activated nitrogen species
generated from a nitrogen-containing plasma effective to introduce nitrogen into
the silicon oxide comprising layer, and forming silicon nitride therefrom, with at
least some silicon oxide remaining within said previously formed pinholes; and
after the exposing, forming second capacitor electrode material over the
substrate.

9. The method of claim 8 wherein said exposing and forming silicon
nitride therefrom transforms an outermost portion of the silicon oxide within the
pinholes to silicon nitride.

10. The method of claim 8 wherein said exposing and forming silicon
nitride therefrom does not form any silicon nitride within the pinholes.

11. The method of claim 8 comprising forming the silicon oxide
comprising layer on the silicon nitride comprising layer.

Sub 3.1

12. The method of claim 8 comprising forming an inner silicon oxide comprising layer on the first capacitor electrode material, with the silicon nitride comprising layer being formed on the inner silicon oxide comprising layer.

13. The method of claim 8 comprising forming the second capacitor electrode on silicon nitride of the capacitor.

14. The method of claim 8 wherein the forming silicon nitride therefrom comprises thermally annealing the substrate at a temperature of at least 600°C after the exposing.

0944310-031E4660

15. A method of forming a capacitor comprising:

forming first capacitor electrode material comprising silicon over a semiconductor substrate;

oxidizing the first capacitor electrode material effective to form a first silicon oxide comprising layer thereon;

forming a silicon nitride comprising layer on the first silicon oxide comprising layer, the silicon nitride comprising layer comprising pinholes formed therein;

after forming the silicon nitride comprising layer, oxidizing the substrate effective to both fill said pinholes with silicon oxide material and form a second silicon oxide comprising layer on the silicon nitride comprising layer;

after filling said pinholes, exposing the second silicon oxide comprising layer to an activated nitrogen species generated from a nitrogen-containing plasma effective to introduce nitrogen into the second silicon oxide comprising layer, and forming outer silicon nitride therefrom, with at least some silicon oxide remaining within said previously formed pinholes; and

after the exposing, forming a second capacitor electrode material on the outer silicon nitride.

16. The method of claim 15 wherein the second silicon oxide comprising layer upon forming thereof includes a portion which is everywhere received elevationally over the silicon nitride comprising layer, said exposing and forming outer silicon nitride therefrom transforming all of said portion to silicon nitride.

Sub B-1

17. The method of claim 15 wherein the second silicon oxide comprising layer upon forming thereof includes a portion which is everywhere received elevationally over the silicon nitride comprising layer, said exposing and forming outer silicon nitride therefrom transforming only an outermost part of said portion to silicon nitride.

18. The method of claim 15 wherein said exposing and forming silicon nitride therefrom transforms an outermost portion of the silicon oxide within the pinholes to silicon nitride.

19. The method of claim 15 wherein said exposing and forming silicon nitride therefrom does not form any silicon nitride within the pinholes.

20. The method of claim 15 wherein the forming silicon nitride therefrom comprises thermally annealing the substrate at a temperature of at least 600°C after the exposing.

21. A method of forming a capacitor dielectric layer comprising:
forming a silicon nitride comprising layer over a substrate;
forming an outer silicon oxide comprising layer over the silicon nitride comprising layer;
providing the substrate with the silicon nitride and the silicon oxide comprising layers within a plasma deposition chamber, the chamber comprising a substrate receiver and a powerable electrode spaced therefrom, the substrate being received by the receiver;
providing a spacing between the receiver and the electrode of at least 0.1 inch, with the substrate being received on the receiver;
with such spacing, injecting a nitrogen comprising gas to within the chamber and with the electrode generating a plasma therefrom effective to form an activated nitrogen species which diffuses into the outer silicon oxide comprising layer, and forming silicon nitride therefrom in only an outermost portion of the silicon oxide comprising layer.
22. The method of claim 21 wherein the generated plasma is spaced from the outer silicon oxide comprising layer.
23. The method of claim 21 wherein the spacing is at least 1.0 inch.
24. The method of claim 21 wherein the spacing is at least 2.0 inches.

25. The method of claim 21 wherein the spacing is at least 4.0 inches.

26. The method of claim 21 wherein the nitrogen comprising gas comprises N_2 .

27. The method of claim 21 wherein the nitrogen comprising gas comprises NH_3 .

28. The method of claim 21 wherein the nitrogen comprising gas comprises NO_x .

29. The method of claim 21 comprising forming the silicon nitride comprising layer to have pinholes formed therein, wherein said diffusing and forming silicon nitride therefrom transforms an outermost portion of the silicon oxide within the pinholes to silicon nitride.

30. The method of claim 21 comprising forming the silicon nitride comprising layer to have pinholes formed therein, wherein said diffusing and forming silicon nitride therefrom does not form any silicon nitride within the pinholes.

106230 03 FEB 90

00443130 03E7650

31. A capacitor comprising:

a first capacitor electrode;

a second capacitor electrode; and

a capacitor dielectric region received intermediate the first and second capacitor electrodes, the capacitor dielectric region comprising a silicon nitride comprising layer having an outermost surface which contacts the second capacitor electrode, said outermost surface consisting essentially of silicon nitride, the silicon nitride comprising layer having a plurality of pinholes therein which are at least partially filled with silicon oxide material which is spaced from the second electrode.

32. The capacitor of claim 31 wherein the pinholes are totally filled with silicon oxide material.

33. The capacitor of claim 31 wherein the pinholes are only partially filled with silicon oxide material.

34. The capacitor of claim 31 wherein the pinholes comprise uppermost portions filled with silicon nitride material.

35. The capacitor of claim 31 wherein the dielectric region comprises an inner silicon oxide comprising layer received intermediate the first capacitor electrode and the silicon nitride comprising layer.

36. A capacitor comprising:
a first capacitor electrode;
a second capacitor electrode; and
a capacitor dielectric region received intermediate the first and second capacitor electrodes, the capacitor dielectric region comprising:

a silicon oxide comprising layer received on the first capacitor electrode; and

a silicon nitride comprising layer received on the silicon oxide comprising layer, the silicon nitride comprising layer having an outermost surface which contacts the second capacitor electrode, said outermost surface consisting essentially of silicon nitride, the silicon nitride comprising layer having a plurality of pinholes therein which are at least partially filled with silicon oxide material which is spaced from the second electrode.

37. The capacitor of claim 36 wherein the pinholes are totally filled with silicon oxide material.

38. The capacitor of claim 36 wherein the pinholes are only partially filled with silicon oxide material.

39. The capacitor of claim 36 wherein the pinholes comprise uppermost portions filled with silicon nitride material.